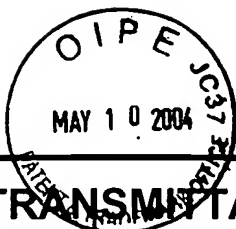


ITW



<b>TRANSMITTAL FORM</b> (to be used for all correspondence after initial filing)		Application No.	10/612,775
		Filing Date	July 2, 2003
		First Named Inventor	Kuo-Hsing Cheng
		Art Unit	2825
		Examiner Name	Thompson, Annette M
Total Number of Pages in This Submission	9	Attorney Docket Number	4728P042D

ENCLOSURES (check all that apply)				
<input checked="" type="checkbox"/> Fee Transmittal Form  <input type="checkbox"/> Fee Attached  <input type="checkbox"/> Amendment / Response  <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s)  <input type="checkbox"/> Extension of Time Request  <input type="checkbox"/> Express Abandonment Request  <input checked="" type="checkbox"/> Information Disclosure Statement <input checked="" type="checkbox"/> PTO/SB/08  <input type="checkbox"/> Certified Copy of Priority Document(s)  <input type="checkbox"/> Response to Missing Parts/Incomplete Application  <input type="checkbox"/> Basic Filing Fee <input type="checkbox"/> Declaration/POA  <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s)  <input type="checkbox"/> Licensing-related Papers  <input type="checkbox"/> Petition  <input type="checkbox"/> Petition to Convert a Provisional Application  <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address  <input type="checkbox"/> Terminal Disclaimer  <input type="checkbox"/> Request for Refund  <input type="checkbox"/> CD, Number of CD(s)	<input type="checkbox"/> After Allowance Communication to Group  <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences  <input type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)  <input type="checkbox"/> Proprietary Information  <input type="checkbox"/> Status Letter  <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): <div style="border: 1px solid black; padding: 5px; margin-top: 5px;">Copies of 21 IDS references; and return postcard</div>		
<table border="1"><tr><td>Remarks</td><td>IDS with Form PTO-892 (Examiner's Notice of References Cited) Part of Paper No. 5</td></tr></table>			Remarks	IDS with Form PTO-892 (Examiner's Notice of References Cited) Part of Paper No. 5
Remarks	IDS with Form PTO-892 (Examiner's Notice of References Cited) Part of Paper No. 5			

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	Eric S. Hyman, Reg. No. 30,139 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	5/1/04

CERTIFICATE OF MAILING/TRANSMISSION			
I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop - DD, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.			
Typed or printed name	Linda D'Elia		
Signature		Date	5-7-04

# FEE TRANSMITTAL for FY 2004

Effective 10/01/2004. Patent fees are subject to annual revision.

☒ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT (\$) 0.00

## Complete if Known

Application Number 10/612,775  
Filing Date July 2, 2003  
First Named Inventor Kuo-Hsing Cheng  
Examiner Name Thompson, Annette M  
Art Unit 2825  
Attorney Docket No. 4728P042D

## METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account

Deposit Account Number 02-2666

Deposit Account Name Blakely, Sokoloff, Taylor & Zafman LLP

The Commissioner is authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Credit any overpayments

☒ Charge any additional fee(s) or underpayment of fees as required under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.

☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account

## FEE CALCULATION

### 1. BASIC FILING FEE

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	
SUBTOTAL (1)					(\$)

### 2. EXTRA CLAIM FEES

Total Claims	Extra Claims	Fee from below	Fee Paid
4	20*	0	9.00 = \$0.00
Independent Claims	4*	0	43.00 = \$0.00
Multiple Dependent			

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1202	18	2202	9	Claims in excess of 20	
1201	86	2201	43	Independent claims in excess of 3	
1203	230	2203	145	Multiple Dependent claim, if not paid	
1204	86	2204	43	**Reissue independent claims over original patent	
1205	18	2205	9	**Reissue claims in excess of 20 and over original patent	
SUBTOTAL (2)					(\$) 0.00

\*or number previously paid, if greater, For Reissues, see below

## FEE CALCULATION (continued)

### 3. ADDITIONAL FEES

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
2053	130	2053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for ex parte reexamination	
1804	920 *	1804	920 *	Requesting publication of SIR prior to Examiner action	
1805	1,840 *	1805	1,840 *	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1404	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	1809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) \_\_\_\_\_

\* Reduced by Basic Filing Fee Paid

SUBTOTAL (3)

(\$)

## SUBMITTED BY

## Complete (if applicable)

Name (Print/Type) Eric S. Hyman Registration No. (Attorney/Agent) 30,139 Telephone (310) 207-3800  
Signature Date 5/16/04

Based on PTO/SB/17 (10-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wtr) 02/10/2004.  
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The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

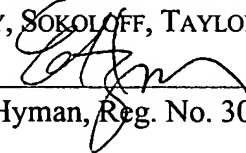
Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: \_\_\_\_\_

5/7/04

  
Eric S. Hyman, Reg. No. 30,139

12400 Wilshire Boulevard, 7th Floor  
Los Angeles, CA 90025  
Telephone: (310) 207-3800

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Linda D'Elia

May 7, 2004

Date



Substitute for form 1449A/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(use as many sheets as necessary)</i>				Application Number	10/612,775
				Filing Date	July 2, 2003
				First Named Inventor	Kuo-Hsing Cheng
				Art Unit	2825
				Examiner Name	Thompson, Annette M
Sheet	1	of	3	Attorney Docket Number	4728P042D

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		SHELDON B. AKERS, "clustering Techniques For Vlsi", CH1681-6/82/0000-0472, 1982 IEEE (pp. 472-476)	
		CHARLES J. ALPERT, et al., "Multilevel Circuit Partitioning", UCLA Computer Science Dept., L.A., CA., (Paper 32.5; pp. 530-533)	
		CHARLES J. ALPERT, et al., "Spectral Partitioning: The More eigenvectors, The Better", UCLA Computer Science Department, L.A., CA., 32nd ACM/IEEE Design Automation Conference (6 pages)	
		JASON CONG, et al., "Large Scale Circuit Partitioning With Loose/Stable Net Removal And Signal Flow Based Clustering", 1092-3152/97, 1997 IEEE (pp. 441-446)	
		JASON CHONG, et al., "Multiway Partitioning with Pairwise Movement", UCLA Dept. of Computer Science, L.A., CA (pp. 512-516)	
		SHANTANU DUTT, et al., "A Probability-Based Approach to VLSI Circuit Partitioning", Dept. of Electrical Engineering, Univ. of Minnesota, Minneapolis, MN (Paper 6.4; pp. 100-104)	
		SHANTANU DUTT, "New Faster Kernighan-Lin-Type Graph-Partitioning Algorithms", Dept. of Electrical Engineering, Univ. of Minnesota, Minneapolis, MN., 1063-6757/93, 1993 IEEE (pp. 370-377)	

Examiner Signature		Date Considered	
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\*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

<sup>1</sup>Applicant's unique citation designation number. <sup>2</sup>Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449A/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(use as many sheets as necessary)</i>				Application Number	10/612,775
				Filing Date	July 2, 2003
				First Named Inventor	Kuo-Hsing Cheng
				Art Unit	2825
				Examiner Name	Thompson, Annette M
				Attorney Docket Number	4728P042D
Sheet	2	of	3		

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		
		C.M. FIDUCCIA et al., "A LINEAR-TIME HEURISTIC FOR IMPROVING NETWORK PARTITIONS", 19TH Design Automation Conference, 0420-0098/82/0000/0175, 1982 IEEE, (Paper 13.1; pp. 175-181)		
		JORN GARBERS, et al., "Finding Clusters In VLSI Circuits", Research Institute of Discrete Mathematics; CH2924-9/90/0000/0520, 1990 IEEE (pp. 520-523)		
		M.R. GAREY, et al., "Computers and Intractability", A2 Network Design (pp. 209-219)		
		MICHAEL R. GAREY, et al., "Computers and Intractability" A guide to the Theory of NP-Completeness, Bell Laboratories (2 pages)		
		LARS HAGEN, et al., "Fast Spectral Methods For Ratio Cut Partitioning and Clustering", UCLA Dept. of Computer Science, L.A., CA. CH3026-2/91/0000/0010, 1991 IEEE (pp. 10-13)		
		MICHAEL A.B. JACKSON, et al., "A Fast Algorithm For Performance-Driven Placement", Electronics Research Lab, Univ. of Calif., Berkeley, CA, CH2924-9/90/0000/0328, 1990 IEEE, (pp. 328-331)		
		B.W. KERNIGHAN, et al., "An Efficient Heuristic Procedure For Partitioning Graphs", Manuscript received September 30, 1969, (pp. 291-307)		

Examiner Signature		Date Considered	
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				Examiner Name	Thompson, Annette M
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		DONALD E. KNUTH, "The Art of Computer Programming", Vol. 3/Sorting and Searching, Addison-Wesley Publ. Company, This book is in the Addison-Wesley Series In Computer Science and Info. Processing, (6 pages)		
		BALAKRISHNAN KRISHNAMURTHY, "An Improved Min-Cut Algorithm For Partitioning VLSI Networks", IEEE Transactions on Computers, Vol. C-33, No. 5, May 1984, (pp. 438-446)		
		YOUSSEF G. SAAB, "A Fast and Robust Network Bisection Algorithm", IEEE Transactions on Computers, Vol. 44, No. 7, July 1995, (pp. 903-913)		
		CARL SECHEN, "VLSI Placement and Global Routing Using Simulated Annealing, Book Series: The Kluwer Int'l Series In Engineering and Computer Science: Vol. 54 (1 page)		
		NAVEED A. SHERWANI, "Algorithms For VLSI Physical Design Automation" Third Edition, Kluwer Academic Publishers, (3 pages)		
		CHUNG-KUAN CHENG, "An Improved Two-Way Partitioning Algorithm With Stable Performance", IEEE Transactions on Computer-Aided Design, Vol. 10, No. 12, December 1991, (pp. 1502-1511)		
		YEN-CHUEN WEI, et al., "Towards Efficient Hierarchical Designs By Ratio Cut Partitioning", Computer Science and Engineering Dept., Univ. of Calif., San Diego, La Jolla, CA. CH2805-0/89/0000/0298, 1989 IEEE, (pp. 298-301)		

Examiner Signature		Date Considered	
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